INTEL iSBX™ BUS SPECIFICATION

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Intel Corporation, 3065 Bowers Avenue, Santa Clara, California 95051

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Intel Corporation
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Intelevision	Micromap	μScope

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A195/580/7K DD

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SECTION 1
GENERAL INFORMATION

1.0 INTRODUCTION

The iSBX bus is a unique interface facilitating on-board expansion with iSBX Multimodule boards. The iSBX bus is derived directly from the on-board CPU bus and, as such, an iSBX Multimodule board plugged into the iSBX bus becomes an integral element of the single board computer. The physical interface between the single board computer and the iSBX Multimodule board is a unique connector designed specifically for the iSBX bus. The iSBX bus is brought out to a female iSBX bus connector on the single board computer and mates with its male equivalent resident on the iSBX Multimodule board (figure 1-1).

The iSBX Multimodule board concept offers a unique design approach to board level users. To date, the designer has had a broad range of single board computers and expansion boards joined together on the Multibus interface. The iSBX Multimodule boards bring a new concept to expansion, providing a product family of smaller modules that can be plugged directly onto the single board computer. In short, the user may now tailor his application directly onboard the single board computer at a minimal cost. In addition, the iSBX Multimodule boards offer maximum performance because they are tightly coupled to the microprocessor through the iSBX bus.

This manual has been prepared for those users who intend to evaluate or design custom iSBX Multimodule board products that will be compatible with Intel base boards. This manual defines the logical, electrical, and mechanical aspects of the iSBX Multimodule boards. The iSBX Multimodule board specifications are defined in a similar way an I/O component would be.

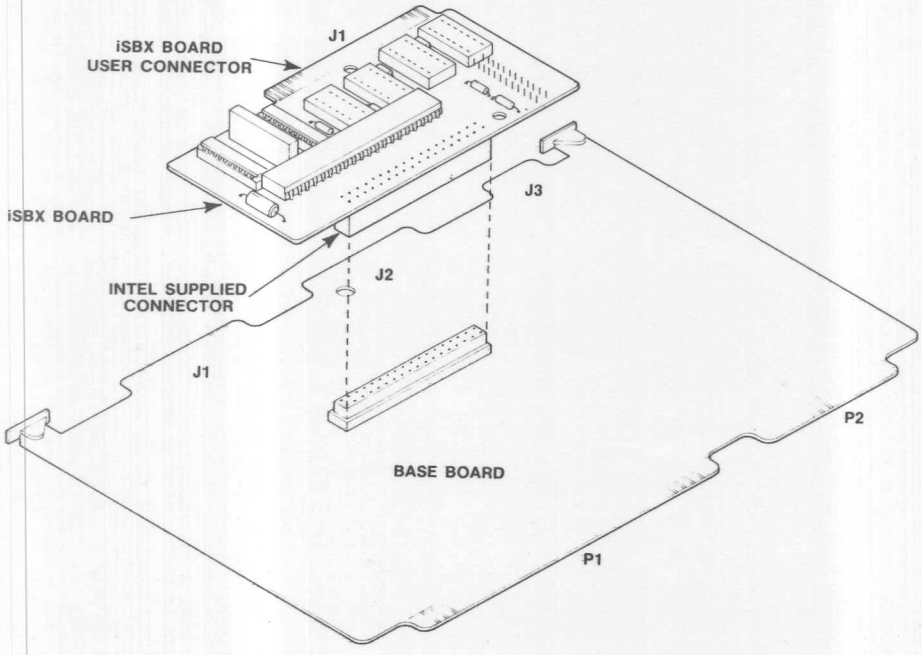


Figure 1-1. iSBX Multimodule Board Concept

SECTION 2
FUNCTIONAL DESCRIPTION

2.0 INTRODUCTION

Section 2 will give the reader an overall understanding of how the iSBX Multimodule board functions. This section describes the basic elements of an iSBX Multimodule board, defines the iSBX Multimodule interface signals and describes the basic communication operations.

In this section, as well as throughout the specification, a clear and consistent notation for signals has been used. The I/O Read (IORD) signal will be used to explain this notation. The terms one, zero, true, and false can be ambiguous, so their use will be avoided. In their place, the terms electrical High and Low (H and L) will be used. A slash following a signal name (IORD/) indicates that the signal is active low as shown:

IORD/ = $\overline{\text{IORD}}$ = IORD− = Asserted at 0 volts

The signal (IORD/), driven by a three state driver, will be pulled up to V_{CC} when not asserted. Table 2-1 is used to further explain the notation used in this specification.

Table 2-1. Notational Summary

Signal Name	Electrical	Definition	
		Logical	State
IORD	H L	1 True 0 False	Active, Asserted
IORD/	L H	1 True 0 False	Active, Asserted

2.1 iSBX MULTIMODULE SYSTEM ELEMENTS

This section will describe the two basic elements in an iSBX Multimodule system; base boards and iSBX Multimodule boards (see figure 1-1).

2.1.1 BASE BOARDS

The base board provides an electrical and mechanical interface for the iSBX Multimodule boards. The electrical interface provides the communication link between the two elements. The base board is the master of this link, in that it controls the address and command signals. The base board also provides the mounting for the iSBX Multimodule board. With the aid of nylon screws, spacers, nuts, and the iSBX connector, the iSBX Multimodule board is mounted to the base board.

There are two classes of base boards, those with Direct Memory Access (DMA) support and without. Base boards with DMA support are boards with DMA controllers on them. These boards, in conjunction with an iSBX Multimodule board (with DMA capability), can perform direct I/O to memory or memory to I/O operations. Base boards without DMA support use a subset of the iSBX bus and simply do not use that aspect of the iSBX Multimodule board.

2.1.2 iSBX MULTIMODULE BOARDS

The iSBX Multimodule boards are small, specialized, I/O mapped boards which plug into base boards. The iSBX boards connect to the iSBX bus connector and convert the iSBX bus signals to a defined I/O interface. An example of an iSBX Multimodule board would be an iSBX 350 Multimodule parallel I/O board. The iSBX 350 Multimodule board converts the iSBX bus signals into 24 buffered I/O lines.

2.2 iSBX BUS INTERFACE

The iSBX bus interface can be grouped into six functional classes:

Control Lines
Address and Chip Select Lines
Data Lines
Interrupt Lines
Option Lines
Power Lines

2.2.1 CONTROL LINES

The following signals are classified as control lines:

COMMANDS:
- IORD/ (I/O Read)
- IOWRT/ (I/O Write)

DMA:
- MDRQT (DMA Reset)
- MDACK/ (DMA Acknowledge)
- TDMA (Terminate DMA)

INITIALIZE:
- RESET

CLOCK:
MCLK (iSBX Multimodule Clock)

SYSTEM CONTROL:
MWAIT/
MPST/ (iSBX Multimodule Board Present)

2.2.1.1 COMMAND LINES (IORD/, IOWRT/). The command lines are active low signals which provide the communication link between the base board and the iSBX Multimodule board. An active command line, conditioned by chip select, indicates to the iSBX Multimodule board that the address lines are valid and the iSBX Multimodule board should perform the specified operation.

2.2.1.2 DMA LINES (MDRQT, MDACK/, TDMA). The DMA lines are the communication link between the DMA controller device on the base board and the iSBX Multimodule board. MDRQT is an active high output signal from the iSBX Multimodule board to the base board's DMA device requesting a DMA cycle. MDACK/ is an active low input signal to the iSBX Multimodule board from the base board DMA device acknowledging that the requested DMA cycle has been granted. TDMA is an active high output signal from the iSBX Multimodule board to the base board. TDMA is used by the iSBX Multimodule board to terminate DMA activity. The use of the DMA lines is optional as not all base boards will provide DMA channels and not all iSBX Multimodule boards will be capable of supporting a DMA channel.

2.2.1.3 INITIALIZE LINES (Reset). This input line to the iSBX Multimodule board is generated by the base board to put the iSBX Multimodule board into a known internal state.

2.2.1.4 CLOCK LINES (MCLK). This input to the iSBX Multimodule board is a timing signal. The 10 MHz (+0%, −10%) frequency can vary from base board to base board. This clock is asynchronous from all other iSBX bus signals. (This is the same specification as BCLK and CCLK in the Multibus Specification.)

2.2.1.5 SYSTEM CONTROL LINES (MWAIT/, MPST/). These output signals from the iSBX Multimodule board control the state of the system.

Active MWAIT/ (Active Low) will put the CPU on the board into a wait state providing additional time for the iSBX Multimodule board to perform the requested operation. MWAIT/ must be generated from address (address plus chip select) information only. If MWAIT/ is driven active due to a glitch on the CS line during address transitions, MWAIT/ must be driven inactive in less than 75 ns.

The iSBX Multimodule board present (MPST/) is an active low signal (tied to signal ground) that informs the base board I/O decode logic that an iSBX Multimodule board has been installed.

2.2.2 ADDRESS AND CHIP SELECT LINES

The address and chip select lines are made up of two groups of signals.

Address Lines:	MA0-MA2
Chip Select Lines:	MCS0/-MCS1/

The base board decodes I/O addresses and generates the chip selects for the iSBX Multimodule boards. The base board decodes all but the lower order three addresses in generating the iSBX Multimodule board chip selects. Thus, a base board would normally reserve two blocks of 8 I/O ports for each iSBX socket it provides.

2.2.2.1 ADDRESS LINES (MA0-MA2). These positive true input lines to the iSBX Multimodule boards are generally the least three significant bits of the I/O address. In conjunction with the command and chip select lines, they establish the I/O port address being accessed.

2.2.2.2 CHIP SELECT LINES (MCS0/-MCS1/). These input lines to the iSBX Multimodule board are the result of the base board I/O decode logic. MCS/ is an active low signal which conditions the I/O command signals and thus enables communication with the iSBX Multimodule boards.

NOTE

If MCS/ glitches, the MWAIT/ line may also glitch. MWAIT/ must be in its proper state in less than t_{CW} (75 ns) after MCS/ is in its proper state.

2.2.3 DATA LINES (MD0-MD7)

Eight bidirectional data lines (active high) are used to transmit or receive information to or from the iSBX Multimodule ports. MD0 is the least significant bit.

2.2.4 INTERRUPT LINES (MINTR0-MINTR1).

These active high output lines from the iSBX Multimodule board are used to make interrupt requests to the base board.

2.2.5 OPTION LINES (OPT0, OPT1)

These two signals are two reserved lines that are connected to wire wrap posts on both the base board

and iSBX Multimodule board. They are for unique requirements where a user needs a base board signal on the iSBX Multimodule board and is willing to put a potentially long wire on the base board to connect it.

2.2.6 POWER LINES

All base boards will provide +5 and ±12 volts to the iSBX Multimodule boards.

2.3 iSBX MULTIMODULE COMMAND OPERATIONS

The command lines are driven from the base board by tri-state drivers with pull-up resistors or standard TTL totem pole drivers. These lines indicate to the iSBX Multimodule board what action is being requested.

2.3.1 I/O READ

There are two I/O READ operations that a base board can perform. The iSBX Multimodule board determines which type of I/O READ is performed.

The first type is a full speed I/O READ (figure 2-1). The base board generates a valid I/O address and a valid chip select for the iSBX Multimodule board. After the set up timings are met, the base board activates the IORD line. The iSBX Multimodule board must generate valid data from the addressed I/O port in less than 250 ns. The base board then reads the data and removes the read command, address, and chip select as shown in the timing diagram.

The second type of I/O READ is an extended read (figure 2-2). This type of read is used by iSBX Multimodule boards that cannot perform a READ operation under the full speed specifications. The base board generates a valid address and chip select, just as in a full speed read. The iSBX Multimodule board then activates the MWAIT/ signal which in turn deactivates the ready input to the CPU (putting it into a WAIT state). The iSBX Multimodule board will remove the MWAIT/ signal when valid READ data is on the iSBX Multimodule data bus. The base board then reads the data and deactivates the command, address, and chip select.

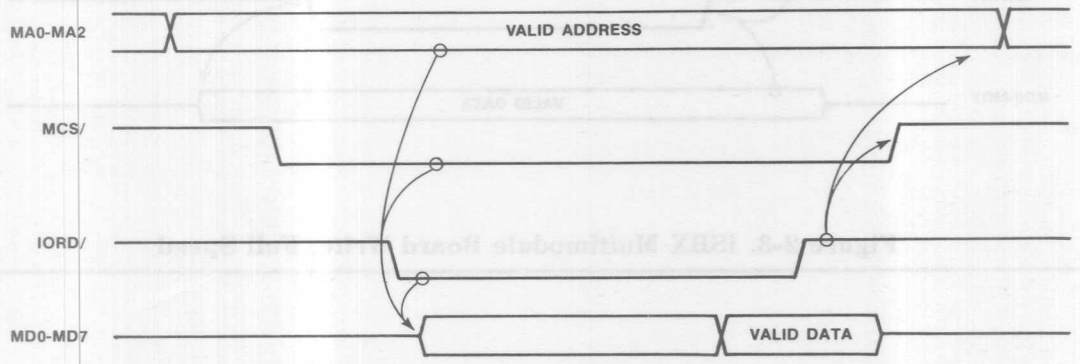


Figure 2-1. iSBX Multimodule Board Read, Full Speed

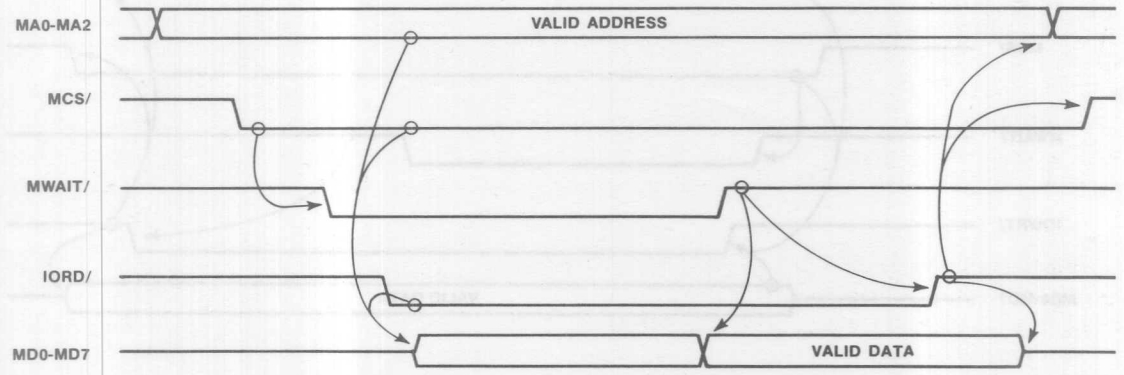


Figure 2-2. iSBX Multimodule Board Extended Read

2.3.2 I/O WRITE

There are two I/O WRITE operations that a base board can perform. The iSBX Multimodule board determines which type of I/O WRITE is performed.

The first type of write is a full speed I/O WRITE (figure 2-3). The base board generates a valid I/O address and chip select. The base board activates the IOWRT line after the set up times are met. The IOWRT/ line will remain active for 300 ns and the data will be valid for 250 ns before the IOWRT/ command is removed. The base board will then remove the data address and chip select after it meets the hold times as shown in figure 2-3.

The second type of I/O WRITE is an extended write (figure 2-4). This write is used by iSBX Multimodule boards that cannot write into an I/O port with the full speed specifications. The base board again generates valid address and chip selects. The iSBX Multimodule board will activate the MWAIT/ signal based on address information (chip select + MA0-1). This will remove the ready from the CPU causing it to go into a wait state after the WRITE command has been activated and valid data provided. The iSBX Multimodule board will remove the MWAIT/ signal (allowing the CPU to leave its wait state) when it has satisfied its write pulse width requirement. The base board will then remove the WRITE command, then the data, address, and chip select after the hold times are met.

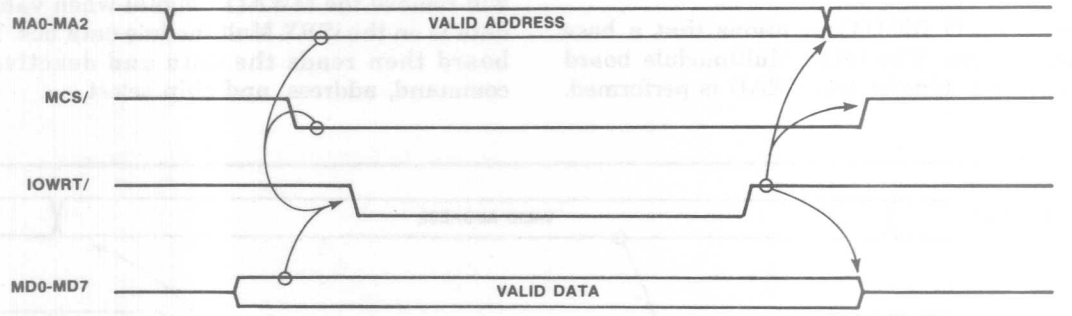


Figure 2-3. iSBX Multimodule Board Write, Full Speed

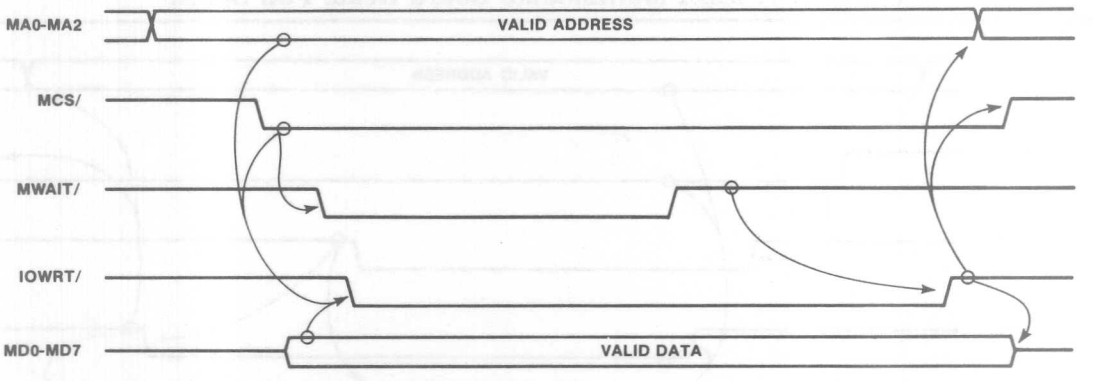


Figure 2-4. iSBX Multimodule Board Extended Write

2.3.3 DIRECT MEMORY ACCESS (DMA)

An iSBX Multimodule system can support DMA when the base board has a DMA controller and the iSBX Multimodule board can support DMA mode. The following example is for a base board using an 8257 DMA controller. Because of the similarity between DMA reads and DMA writes, only the DMA write is given in the following example. A DMA cycle is initiated when the iSBX Multimodule board activates MDRQT, which goes to the DMA controller on the base board (figure 2-5). Once the DMA controller gains control of the base board bus, it acknowledges back to the iSBX Multimodule board with MDACK/. The DMA controller then activates a memory write or I/O write respectively. The delay may be zero, if the memory is a trailing edge type (data is written when the write pin changes from active to inactive state). The MDACK/ signal must act as a chip select and address to the iSBX Multimodule board (the MCS and MA0-MA1 signals are undetermined as they are driven by the memory address). The iSBX Multimodule board will remove the DMA request during the cycle to stop the DMA cycle. Once the write operation is complete (MWAIT inactive and memory acknowledge active), the DMA controller deactivates the write command and the read command providing a data hold time. If the DMA request signal was removed, the controller will release the base board bus back to the CPU and remove MDACK/. If the request is not removed, the DMA controller will procede to do another DMA cycle (burst mode).

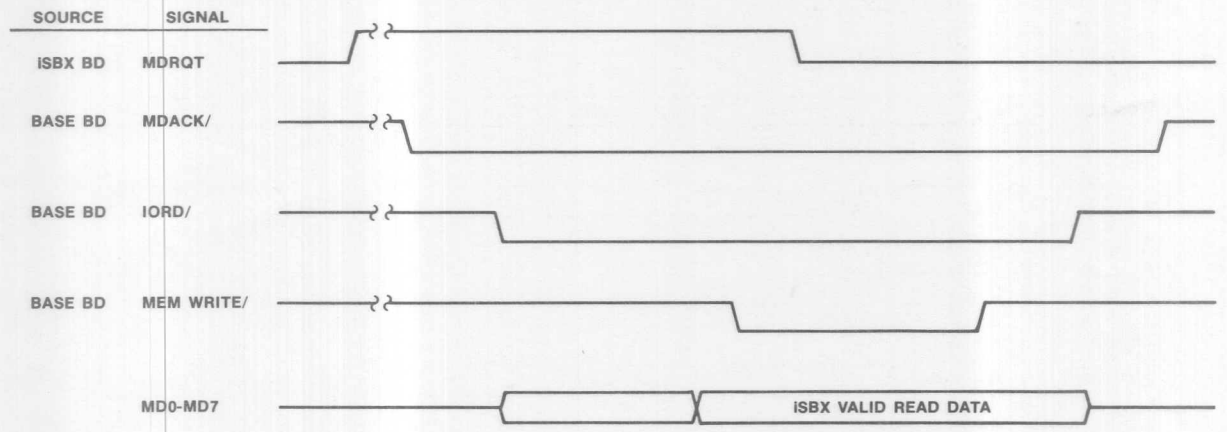


Figure 2-5. iSBX Multimodule Board DMA Cycle (iSBX Multimodule to Base Board Memory)

SECTION 3
ELECTRICAL SPECIFICATIONS

3.0 INTRODUCTION

This section will define all electrical specifications for an iSBX Multimodule board. First the ac timing is specified and then the dc specifications are described.

3.1 GENERAL BUS CONSIDERATIONS

Table 3-1 shows the relationship between logical and electrical states.

3.2 POWER SUPPLY SPECIFICATIONS

All power supply voltages are ±5%.

Minimum (volts)	Nominal (volts)	Maximum (volts)	Maximum (current)*
+4.75	+5.0	+5.25	3.0A
+11.4	+12	+12.6	1.0A
−12.6	−12	−11.4	1.0A
—	GND	—	6.0A

* Per iSBX Multimodule board mounted on base board.

3.3 ENVIRONMENTAL

All bus specifications should be met while the environment is within the following ranges:

Temperature: 0-55°C (32-131°F)
Free moving air across the base board and iSBX Multimodule board.

Humidity: 90% max relative (no condensation).

Shock: 30 g's of force for an 11 msec duration 3 times in 3 planes both sides (total of 18 drops).

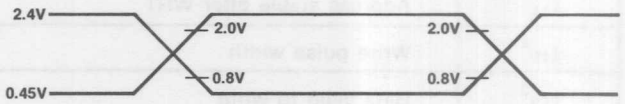
Vibration: Sweeping from 10 Hz to 55 Hz and back to 10 Hz at a distance of 0.010 inches peak-to-peak lasting 15 minutes in each of three planes.

3.4 TIMING

Table 3-2 summarizes all the ac timing specifications. The timing diagrams are shown in figures 3-1 through 3-4.

NOTE

The input waveforms for the ac timing specifications are as follows:



3.5 DC SPECIFICATIONS

The dc specifications for the iSBX bus are summarized in table 3-3. The table is divided into two sections, output specifications and input specifications. The output specifications are the requirements

Table 3-1. Logical and Electrical States

Signal Name	Logical State	Electrical Signal Level	At Receiver	At Driver
IORD/	0	H = TTL High State	5.25 ≥ H ≥ 2.0V	5.25 ≥ H ≥ 2.4V
IORD/	1	L = TTL Low State	0.8 ≥ L ≥ −0.5V	0.5 ≥ L ≥ 0V
IORD	0	L = TTL Low State	0.8 ≥ L ≥ −0.5V	0.5 ≥ L ≥ 0V
IORD	1	H = TTL High State	5.25 ≥ H ≥ 2.0V	5.25 ≥ H ≥ 2.4V

V_{CC} = 5 volts ±5% referenced to logical ground.
V = volts.

on the output drivers of the iSBX Multimodule board. (i.e., the data bus output drivers must guarantee at least 1.6 mA @ 0.5 volts.) The output specifications in table 3-3 are the minimum drive requirements. The input specifications are the requirements of the receivers on the iSBX Multimodule board. (e.g., the loading of the address lines (MA0-MA2) can be no greater than 0.5 mA @ 0.8 volts.) Table 3-3 also summarizes the maximum loading permitted on an iSBX Multimodule interface at any one time.

Table 3-2. iSBX Multimodule Board I/O AC Specifications

Symbol	Parameter	Min (ns)	Max (ns)	Figure Reference
t_1	Address stable before read	50	—	3-2
t_2	Address stable after read	30	—	3-2
t_3	Read pulse width	300	—	3-2
t_4[2]	Data valid from read	0	250	3-2
t_5[2]	Data float after read	0	150	3-2
t_6	Time between RD and/or WRT	—	Note 3	
t_7	CS stable before CMD	25	—	3-2
t_8	CS stable after CMD	30	—	3-2
t_9	Power up reset pulse width	50 Msec	—	3-4
t_{10}	Address stable before WRT	50	—	3-1
t_{11}	Address stable after WRT	30	—	3-1
t_{12}[2]	Write pulse width	300	—	3-1
t_{13}[2]	Data valid to write	250	—	3-1
t_{14}	Data valid after write	30	—	3-1
t_{15}	MCLK cycle	100	110	3-4
t_{16}	MCLK width	35	65	3-4
t_{17}[1]	MWAIT/ pulse width	0	4 msec	3-1, 3-2
t_{18}	Reset pulse width	10 Msec	—	3-4
t_{19}	MCS/ to MWAIT/ valid	0	75	3-1, 3-2
t_{20}	DACK set up to I/O CMD	100	—	3-3
t_{21}	DACK hold	30	—	3-3
t_{22}	CMD to DMA RQT removed to end of DMA cycle	—	200	3-3
t_{23}	TDMA pulse width	500	—	3-3
t_{24}[1]	MWAIT/ to valid read data	—	0	3-2
t_{25}[1]	MWAIT/ to WRT CMD	0	—	3-1

NOTES:
1. Required only if WAIT is activated.
2. If MWAIT/ not activated.
3. To be specified by each iSBX Multimodule board.

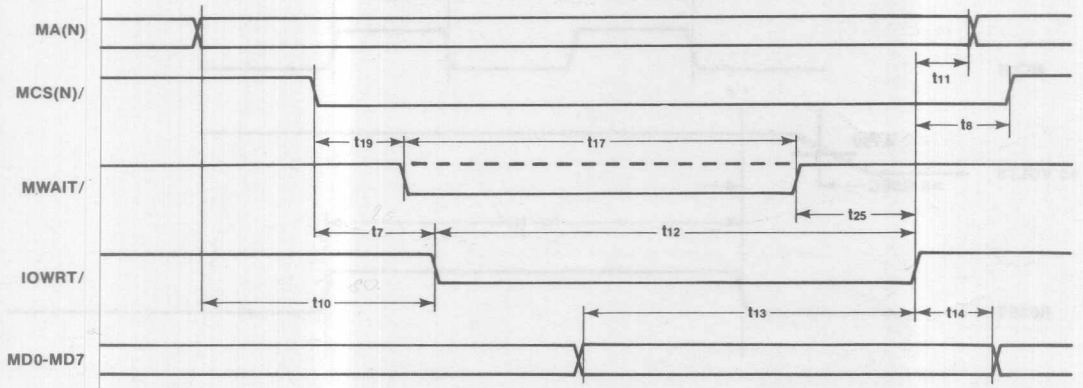


Figure 3-1. iSBX Multimodule Board I/O Write Timing

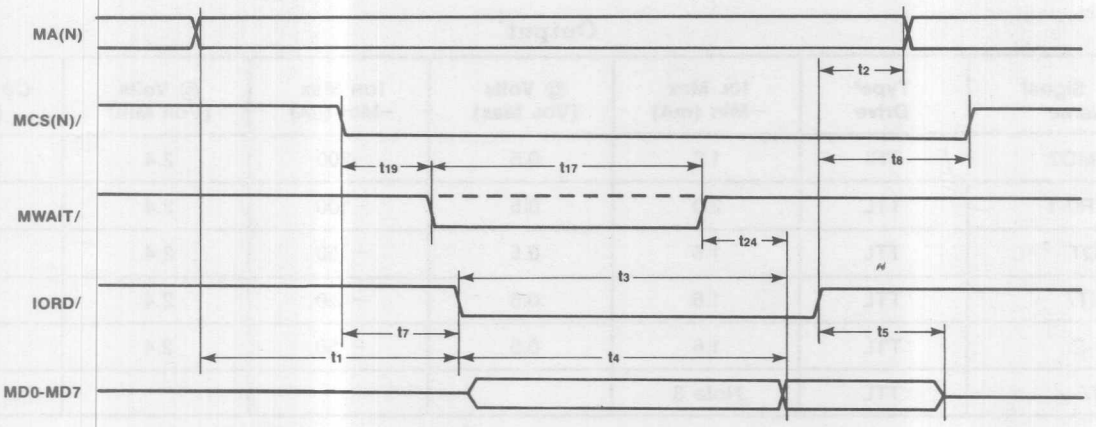


Figure 3-2. iSBX Multimodule Board I/O Read Timing

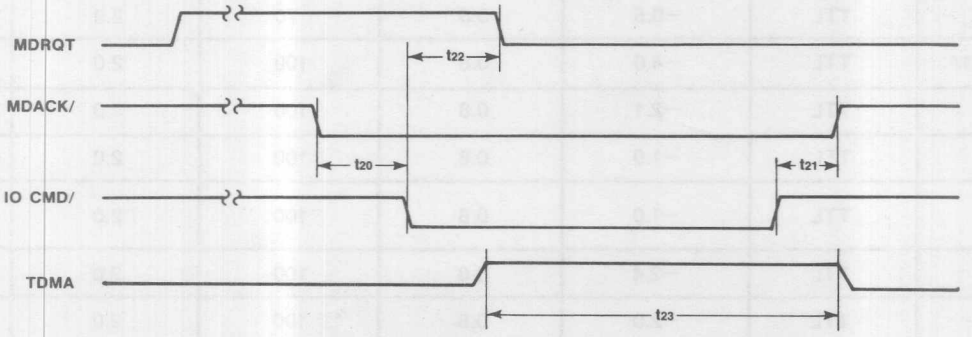


Figure 3-3. iSBX Multimodule Board I/O DMA Timing

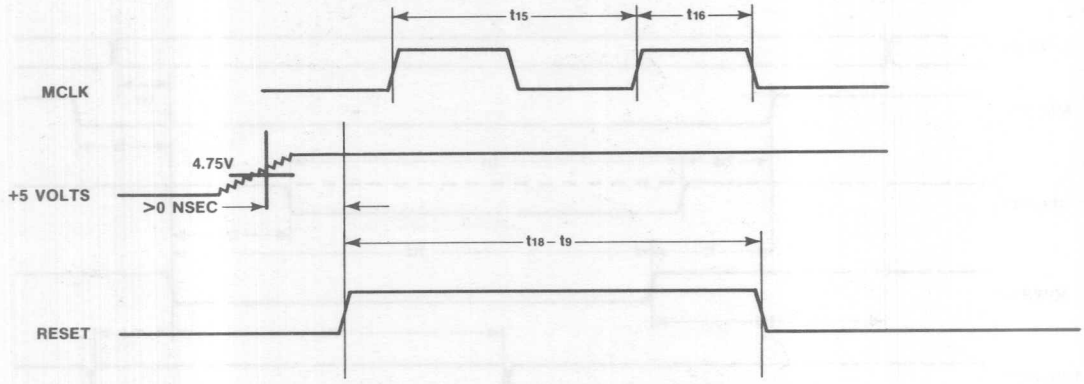


Figure 3-4. iSBX Multimodule Board I/O Reset Timing

Table 3-3. iSBX Multimodule Board I/O DC Specifications

Output[1]

Bus Signal Name	Type[2] Drive	I_{OL} Max —Min (mA)	@ Volts (V_{OL} Max)	I_{OH} Max —Min (μA)	@ Volts (V_{OH} Min)	C_O (Min) (pf)
MD0-MD7	TRI	1.6	0.5	—200	2.4	130
MINTR0-1	TTL	2.0	0.5	—100	2.4	40
MDRQT	TTL	1.6	0.5	— 50	2.4	40
MWAIT/	TTL	1.6	0.5	— 50	2.4	40
OPT1-2	TTL	1.6	0.5	— 50	2.4	40
MPST/	TTL	Note 3				

Input[1]

Bus Signal Name	Type[2] Receiver	I_{IL} Max (mA)	@ V_{IN} Max (volts)	I_{IH} Max (μA)	@ V_{IN} Max (volts)	C_I Max (pf)
MD0-MD7	TRI	—0.5	0.8	70	2.0	40
MA0-MA2	TTL	—0.5	0.8	70	2.0	40
MCS0/-MCS1/	TTL	—4.0	0.8	100	2.0	40
MRESET	TTL	—2.1	0.8	100	2.0	40
MDACK/	TTL	—1.0	0.8	100	2.0	40
IORD/ IOWRT/	TTL	—1.0	0.8	100	2.0	40
MCLK	TTL	—2.4	0.8	100	2.0	40
OPT1-OPT2	TTL	—2.0	0.8	100	2.0	40

NOTES:
1. Per iSBX Multimodule I/O board.
2. TTL = standard totem pole output. TRI = Three-state.
3. iSBX Multimodule board must connect this signal to ground.

SECTION 4
MECHANICAL SPECIFICATIONS

4.0 INTRODUCTION

This section describes all the physical attributes of an iSBX Multimodule board.

4.1 iSBX CONNECTOR

The iSBX connector is a custom made connector that is supplied by Intel. The male iSBX connector is attached to the iSBX Multimodule board and the female iSBX connector is attached to the base board. Figure 4-1 is an outline drawing of the iSBX connector and also shows the pin numbering. Table 4-1 lists the signal pin assignments.

4.2 iSBX MULTIMODULE BOARD HEIGHT REQUIREMENT

Figure 4-2 shows the iSBX Multimodule board height requirements. The total board height minus the iSBX connector is:

Maximum component height (0.400 Max)	0.400
P.C. board thickness (0.62 ±0.005)	0.067
Component lead length (0.093 Max)	0.093
	0.560 in.

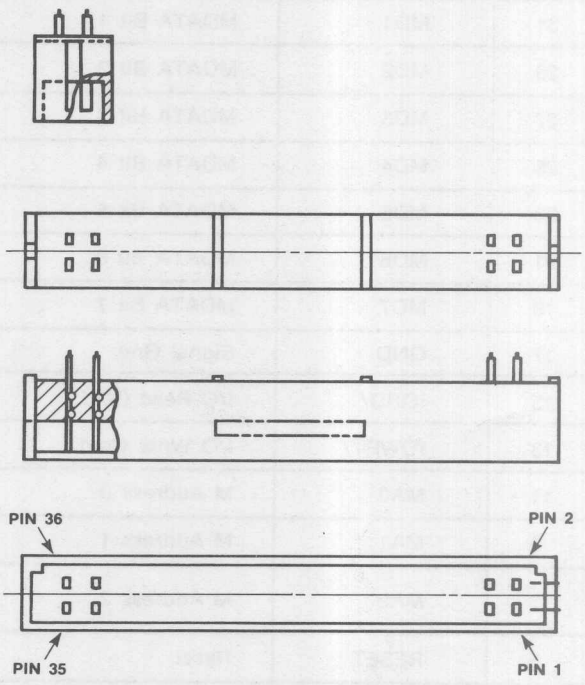


Figure 4-1. iSBX Connector

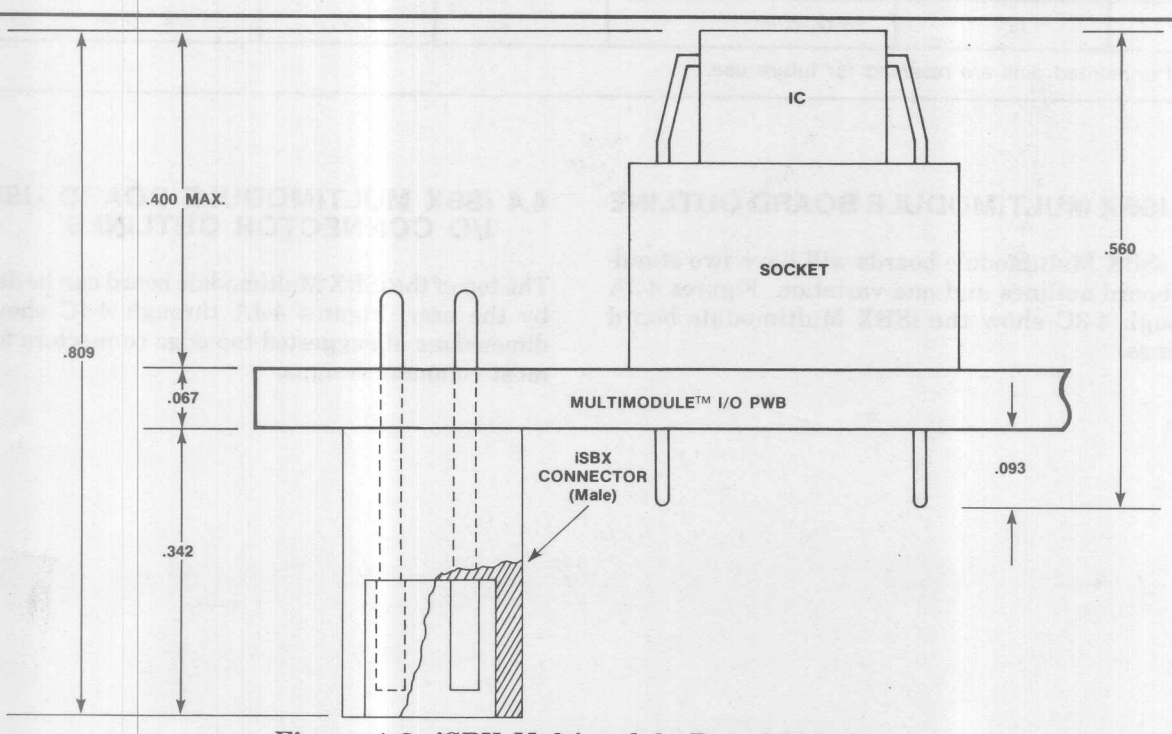


Figure 4-2. iSBX Multimodule Board Height

Table 4-1. iSBX Signal Pin Assigments

Pin	Mnemonic	Description	Pin	Mnemonic	Description
35	GND	Signal Ground	36	+5V	+5 Volts
33	MD0	MDATA Bit 0	34	MDRQT	M DMA Request
31	MD1	MDATA Bit 1	32	MDACK/	M DMA Acknowledge
29	MD2	MDATA Bit 2	30	OPT0	Option 0
27	MD3	MDATA Bit 3	28	OPT1	Option 1
25	MD4	MDATA Bit 4	26	TDMA	Terminate DMA
23	MD5	MDATA Bit 5	24		Reserved
21	MD6	MDATA Bit 6	22	MCS0/	M Chip Select 0
19	MD7	MDATA Bit 7	20	MCS1/	M Chip Select 1
17	GND	Signal Gnd	18	+5V	+5 Volts
15	IORD/	I/O Read Cmd	16	MWAIT/	M Wait
13	IOWRT/	I/O Write Cmd	14	MINTR0	M Interrupt 0
11	MA0	M Address 0	12	MINTR1	M Interrupt 1
9	MA1	M Address 1	10		Reserved
7	MA2	M Address 2	8	MPST/	iSBX Multimodule Board Present
5	RESET	Reset	6	MCLK	M Clock
3	GND	Signal Gnd	4	+5V	+5 Volts
1	+12V	+12 Volts	2	−12V	−12 Volts
All undefined pins are reserved for future use.					

4.3 iSBX MULTIMODULE BOARD OUTLINE

The iSBX Multimodule boards will have two standard board outlines and one variation. Figures 4-3A through 4-3C show the iSBX Multimodule board outlines.

4.4 iSBX MULTIMODULE BOARD USER I/O CONNECTOR OUTLINES

The top of the iSBX Multimodule board can be defined by the user. Figures 4-4A through 4-4C show the dimensions of suggested top edge connectors for the most common designs.

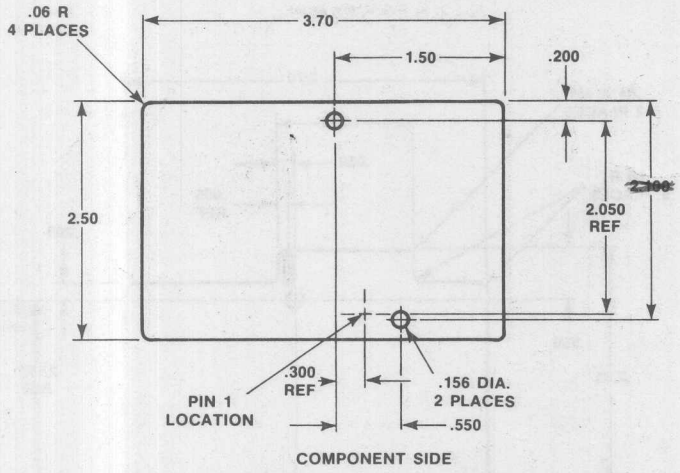


Figure 4-3A. iSBX Multimodule Board Outline OMS #4303064

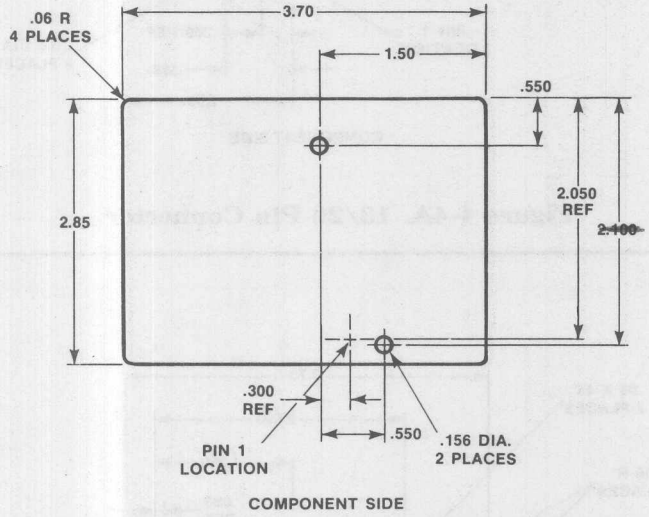


Figure 4-3B. iSBX Multimodule Board Outline OMS #34303076

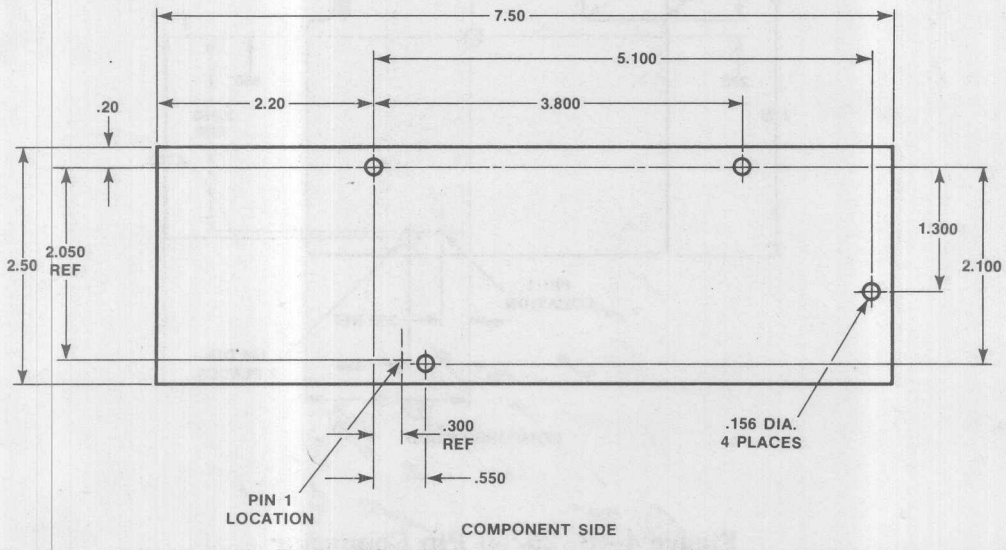


Figure 4-3C. Double Wide iSBX Multimodule Board Outline OMS #4303132

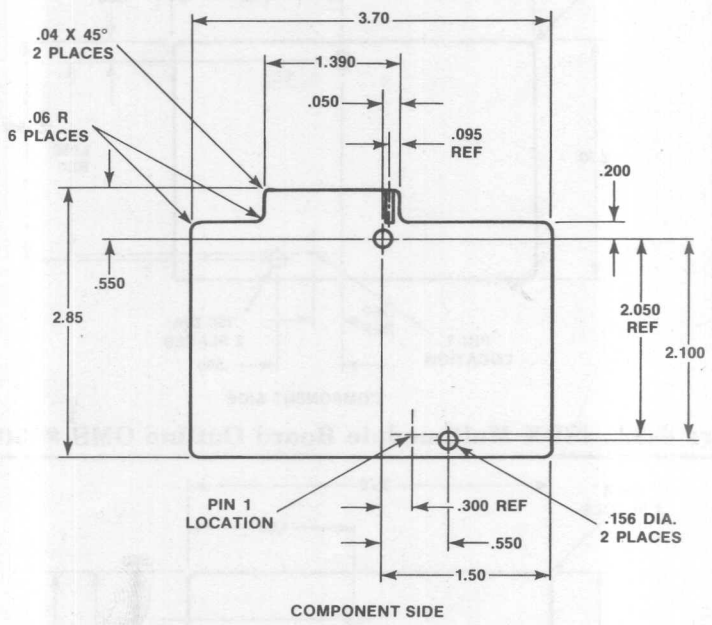


Figure 4-4A. 13/26 Pin Connector

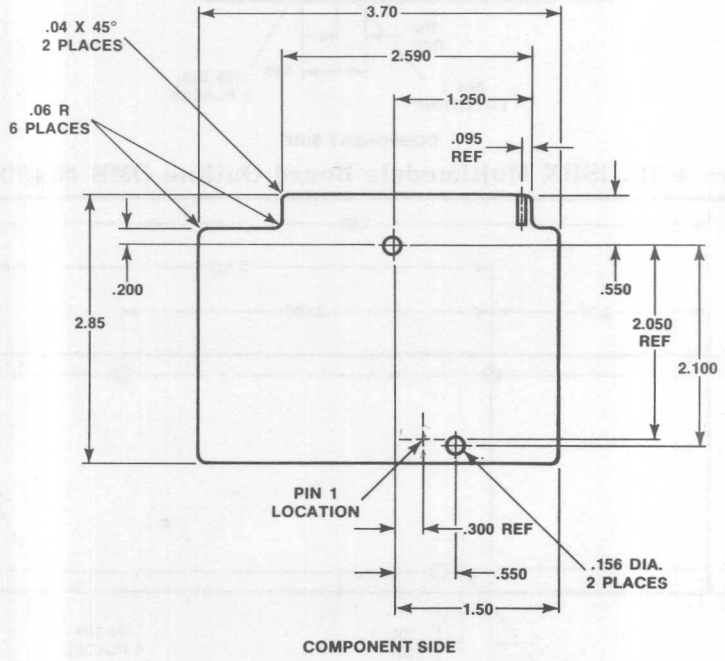


Figure 4-4B. 25/50 Pin Connector

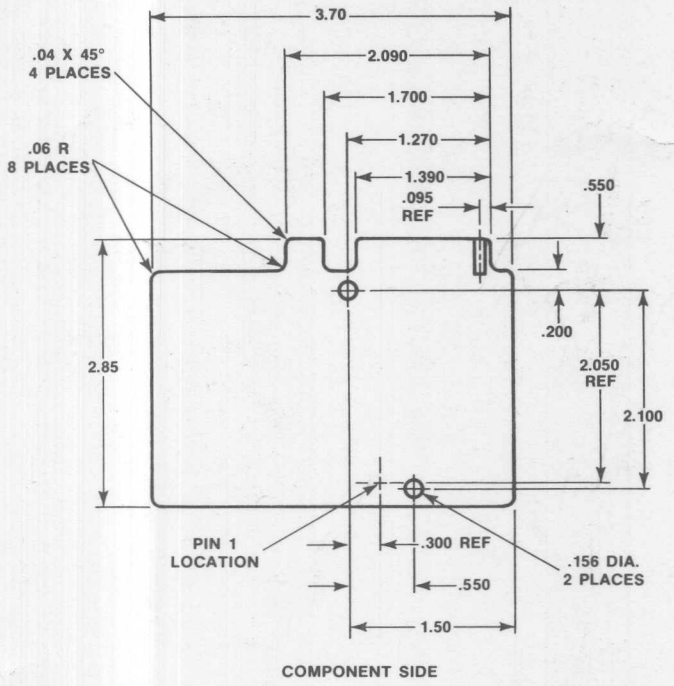


Figure 4-4C. 13/26 and 20/40 Pin Connector

SECTION 5
DESIGN EXAMPLE

5.0 INTRODUCTION

This section provides a functional description of a design example. The design example that will be used is an iSBX 351 Serial Multimodule Board. The functional description includes details on the RS232C and RS422/449 communications interface signals, the interface signals between the iSBX Multimodule board and the host iSBC microcomputer, and the clock generation hardware on the iSBX Multimodule board. Figure 5-1 shows a block diagram of the iSBX Multimodule board.

5.1 SERIAL I/O COMMUNICATIONS CHANNEL INTERFACE

The communications interface on the iSBX Multimodule board may be configured for either RS232C or RS422/449 operation via jumper modifications.

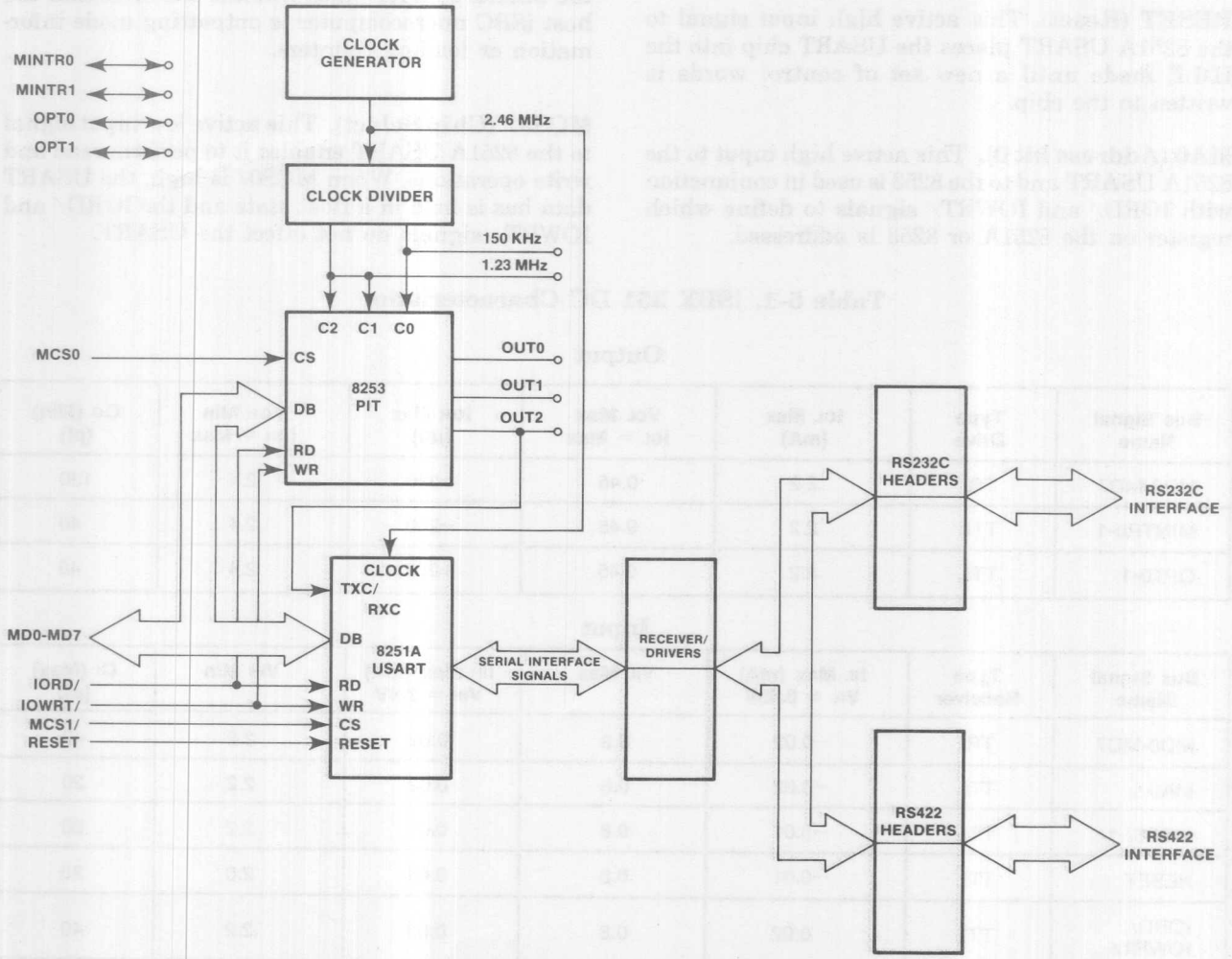


Figure 5-1. iSBX Board Block Diagram

Default wiring of the iSBX Multimodule board is for RS232C operation. To convert to RS422/449 operation, move the two 8-circuit shorting plugs from sockets XU6 and XU7 to XU4 and XU5.

The serial interface provides RS232C or RS422 buffers for eight lines. These lines are the Data In, Data Out, Request to Send, Clear to Send, Data Set Ready, Data Terminal Ready, Receive Clock, and DTE Transmit Clock. All necessary driver and receiver chips are supplied with the board.

5.2 CPU INTERFACE

The interface between the host iSBC microcomputer and the iSBX Multimodule board consists of several signals that are defined in the following paragraphs. The DC characteristics for these signals is given in table 5-1.

RESET (Reset). This active high input signal to the 8251A USART places the USART chip into the IDLE mode until a new set of control words is written to the chip.

MA0 (Address bit 0). This active high input to the 8251A USART and to the 8253 is used in conjunction with IORD/ and IOWRT/ signals to define which register on the 8251A or 8253 is addressed.

MA1 (Address bit 1). This active high input signal to the 8253 is used in conjunction with MA0 to select one of the counters to be operated on in the 8253 and to address the control word register for mode selection.

IORD/ (I/O Read). This active low input signal to the iSBX Multimodule board performs one of two functions depending on the chip selected. When low, IORD/ informs the 8251A that the host iSBC microcomputer is reading data or status from the 8251A, and it informs the 8253 that the host iSBC microcomputer is reading the value of a counter.

IOWRT/ (I/O Write). This active low input to the iSBX Multimodule board may perform one of two functions dependent on chip select. When low, IOWRT/ informs the 8251A that the host iSBC microcomputer is writing data or control words to the 8251A. IOWRT/ also informs the 8253 that the host iSBC microcomputer is outputting mode information or loading counters.

MCS0/ (Chip Select). This active low input signal to the 8251A USART enables it to perform read and write operations. When MCS0/ is high, the USART data bus is held in a float state and the IORD/ and IOWRT/ signals do not effect the USART.

Table 5-1. iSBX 351 DC Characteristics

Output

Bus Signal Name	Type Drive	I_{OL} Max (mA)	V_{OL} Max I_{OL} = Max	I_{OH} Max (μA)	V_{OH} Min I_{OH} = Max	C_O (Min) (pf)
MD0-MD7	TRI	2.2	0.45	−390	2.4	130
MINTR0-1	TTL	2.2	0.45	−200	2.4	40
OPT0-1	TTL	2.2	0.45	−200	2.4	40

Input

Bus Signal Name	Type Receiver	I_{IL} Max (mA) V_{IL} = 0.45V	V_{IL} Max	I_{IH} Max (mA) V_{IH} = 2.4V	V_{IH} Min	C_I (Max) (pf)
MD0-MD7	TRI	−0.02	0.8	0.02	2.2	40
MA0-1	TTL	−0.02	0.8	0.02	2.2	20
MCS0/-1/	TTL	−0.01	0.8	0.01	2.2	20
RESET	TTL	−0.01	0.8	0.02	2.0	20
IORD/, IOWRT/	TTL	0.02	0.8	0.02	2.2	40
OPT0-1	TTL	−1.6	0.8	0.02	2.2	40

TTL = Standard totem pole output.
TRI = Three state output.

MCS1/ (Chip Select). This active low input signal to the 8253 PIT enables it to perform read and write operations. However, MCS1/ has no effect on the operation of the internal counters in the 8253.

MD0-MD7 (Bidirectional Data Bus). These active high I/O lines are the iSBX Multimodule boards' tie-in to the host iSBC microcomputer data bus. MD0 through MD7 transfer data, commands, and status between the iSBX Multimodule board and the host iSBC microcomputer.

MINTR0, MINTR1 (Interrupt Request Lines). These active high output lines may be jumpered to OUT 0, or OUT 1 on the 8253, or to TXRDY on the 8251A.

OPT0, OPT1 (Option Lines). These active high I/O lines are included to give the iSBX Multimodule board greater functional flexibility. These lines may be user-configured for special functions.

5.3 INTERFACE BUFFERING

Interface buffering is provided by three receiver/driver logic elements U1, U2, and U3. U1 is an input buffer that may be used with either RS232C or RS442 configuration, depending on the position of the mode selection header blocks. U2 provides RS422 output buffering, and U3 provides RS232C output buffering.

5.4 CLOCK GENERATION CIRCUITRY

The iSBX 351 board includes an 8224 Clock Generator chip that creates a 2.46 MHz output from a 22.1148 MHz crystal input. The output is then passed through a synchronous four-bit counter which generates a 1.23 MHz clock and a 153.6 KHz clock to drive the 8253 PIT. The clock output frequency labeled OUT 2, which is produced by the 8253 PIT, will vary according to the configuration and programming of the PIT chip.

The two remaining clock frequencies output from the 8253 PIT are jumper selectable to generate interrupts for the iSBX Multimodule board.

5.5 AC SPECIFICATIONS

The ac specifications for the iSBX 351 Serial Multimodule Board are listed in Table 5-2. Figures 5-2 and 5-3 define the timing parameters for the iSBX 351 board.

Table 5-2. AC Specifications

Symbol	Parameter	Min (ns)	Max (ns)
t_1	Address stable before IORD/	50	—
t_2	Address stable after IORD/	30	—
t_3	READ pulse width	300	—
t_4	Data valid from IORD/	—	250
t_5	Data float after IORD/	0	100
t_6 (1)	Time between commands	1000	—
t_7	CS stable before CMD	25	—
t_8	CS stable after CMD	30	—
t_9	Address stable before IOWRT/	50	—
t_{10}	Address stable after IOWRT/	30	—
t_{11}	WRITE pulse width	300	—
t_{12}	Data valid to IOWRT/	250	—
t_{13}	Data valid after IOWRT/	30	—
t_{14}	Reset pulse width	2.9 msec	—

NOTES:
1. During initialization, all writes to the control port: t_6 = 1.92 μs. After initialization in asynchronous mode all writes to the control port: t_6 = 2.56 μs. After initialization in synchronous mode all writes to the control port: t_6 = 5.12 μs. All writes to the data port: Depends upon the baud rate since TXRDY must be true.

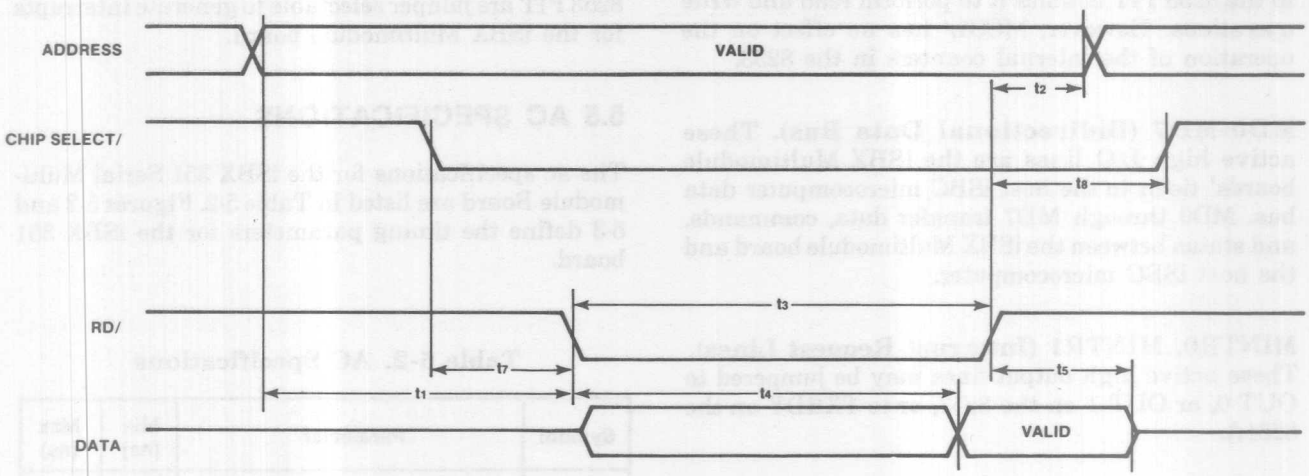


Figure 5-2. READ Timing

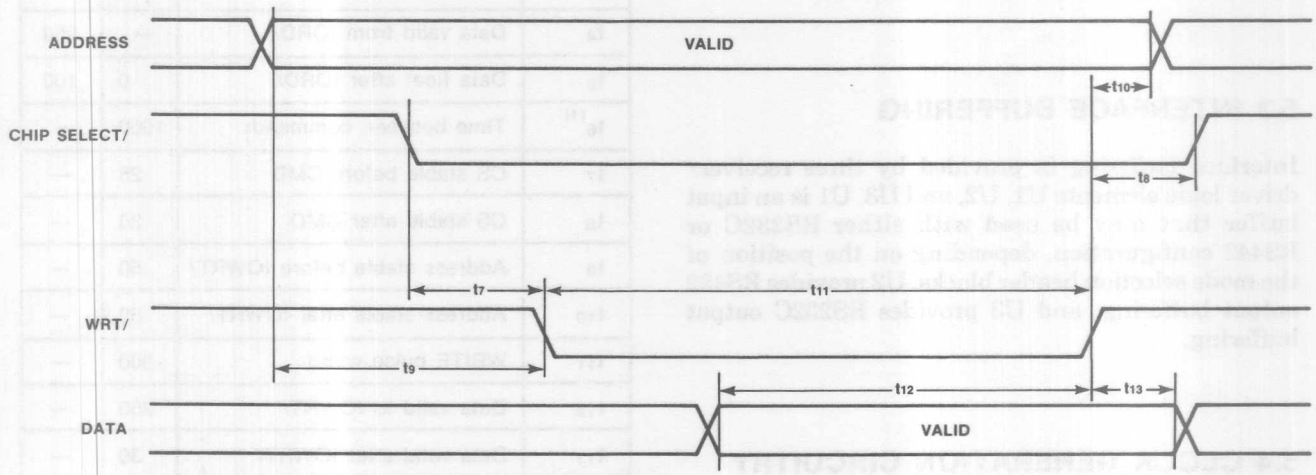


Figure 5-3. WRITE Timing

APPENDIX A
BOARD HEIGHT MOUNTING TECHNIQUES

Figure A-1 shows all component height requirements associated with iSBX Multimodule boards. The total height of a base board and iSBX Multimodule board is 1.127 inches. The elements of this height are as follows:

Component lead length (Solder side base board) (0.90 Typ)	0.093 (Max)
Base board P.C. (0.062 ±0.005)	0.067 (Max)
Base board to iSBX Multimodule board Spacing	0.500
iSBX Multimodule board P.C. (0.062 ±0.005)	0.067 (Max)
Component height of iSBX Multimodule board	0.400 (Max)
	1.127 inches

The iSBX Multimodule board and base board will be mechanically connected together in two places. These two points are the iSBX connector and a nylon screw/spacer assembly. The screw is a 6-32 x ¼ inch and the spacer is ½ inch long.

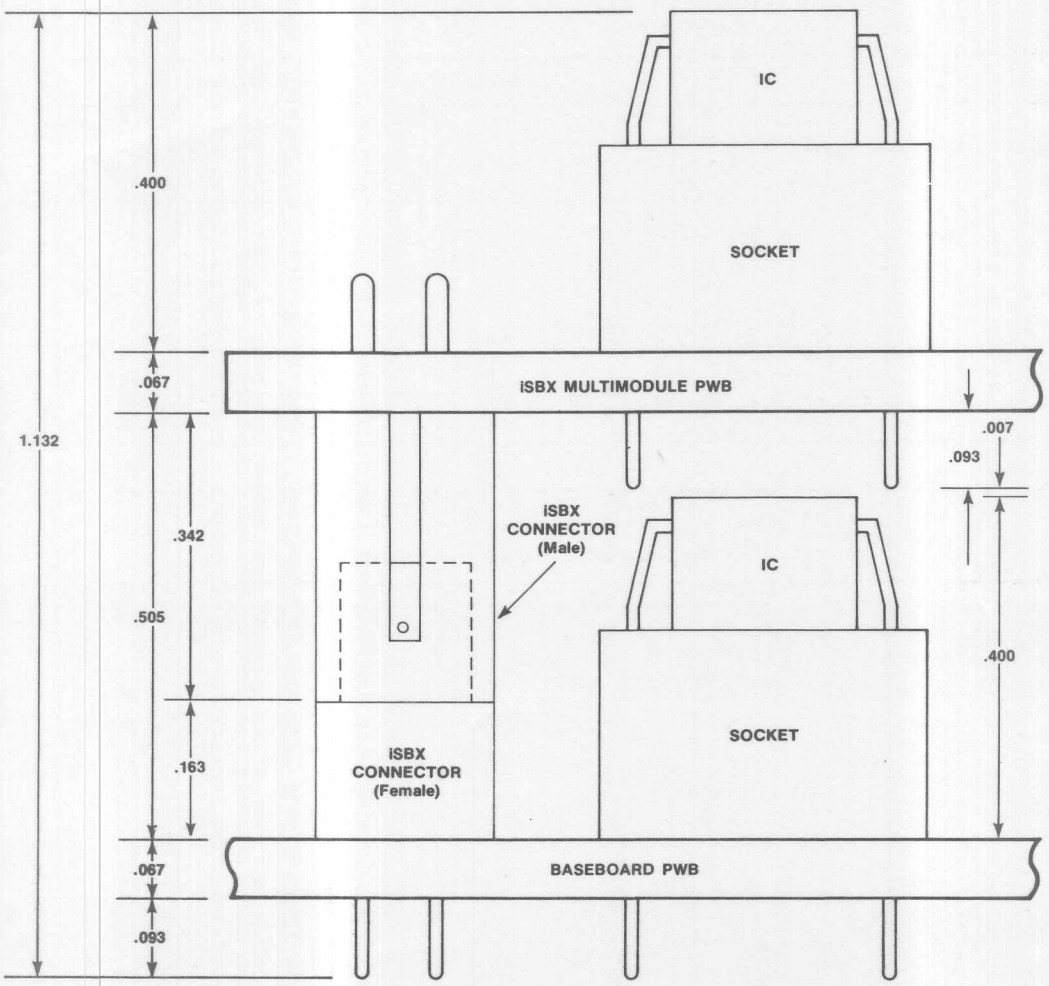


Figure A-1. Component Height Outline